IN THE SPECIFICATION:

Please amend the first paragraph on page two as follows:

This application is a divisional of application Serial No. 09/625,144, filed July 25, 2000, ~~pending~~now U.S. Patent 6,537,922, issued March 25, 2003, which is a continuation of application Serial No. 09/102,152, filed June 22, 1998, now U.S. Patent 6,117,791 issued September 12, 2000.

Please amend the paragraph bridging pages 10 and 11 as follows:

Referring to FIGs. 1 to 4, the etch process of the present invention, which utilizes the inventive etchant, is illustrated. FIG. 1 depicts an exemplary multi-layer structure 10, which is also referred to as a semiconductor device structure, that may be fabricated in part in accordance with the process of the present invention. Multi-layer structure 10 includes a semiconductor substrate 12 (e.g., a silicon wafer, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), silicon-on-glass (SOG), etc.), a field oxide layer 14 that is disposed on an active surface 13 of the semiconductor substrate and an active device region 16, polysilicon lines 18 disposed on the active device region, side wall spacers 20 positioned on each side of the polysilicon lines, an intermediate structural layer 22 disposed over each of the foregoing elements, and a passivation layer 24 disposed over the intermediate ~~structure layer~~ structural layer 22. Passivation layer 24 is fabricated from doped silicon dioxide, such as BPSG, PSG or BSG. Intermediate structural layer 22 may be fabricated from either silicon nitride or undoped silicon dioxide.